

**ABSTRACT**

A method for testing in parallel several identical integrated circuit chips with an asynchronous operation, via two physical contacts between a tester and each of the chips, including transmitting on the tester side a first test control signal for the integrated  
5 circuit chips, having the test executed in desynchronized fashion by each of the integrated circuit chips, transmitting on the tester side, after a predetermined time interval following the transmission of the first control signal, a second result request control signal to the integrated circuit chips, and having all chips respond synchronously upon reception of said second control signal.